

WHAT IS CLAIMED IS:

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1. A charge pump circuit comprising:  
a first transistor;  
a first capacitor coupled to the first transistor;  
a second transistor coupled to the first transistor; and  
a second capacitor coupled to the second transistor, wherein the second transistor has a lower threshold voltage than the first transistor at a common source voltage
2. The charge pump circuit of claim 1 further comprising:  
a third transistor coupled to the second transistor; and  
a third capacitor coupled to the third transistor, wherein the third transistor has a lower threshold voltage than the first transistor at a common source voltage.
3. The charge pump circuit of claim 2 further comprising:  
a fourth transistor coupled to the third transistor; and  
a fourth capacitor coupled to the fourth transistor, wherein the fourth transistor has a lower threshold voltage than the first transistor at a common source voltage.
4. The charge pump circuit of claim 3 further comprising:  
a fifth transistor coupled to the fourth transistor; and  
a fifth capacitor coupled to the fifth transistor, wherein the fifth transistor has a lower threshold voltage than the first transistor at a common source voltage.
5. The charge pump circuit of claim 3 further comprising four diode-connected transistors, wherein each diode-connection transistor is coupled to a gate of one of the first, second, third, and fourth transistors.
6. The charge pump circuit of claim 4 further comprising:  
a sixth transistor coupled to the fifth transistor;  
a sixth capacitor coupled to the sixth transistor;  
a seventh transistor coupled to the sixth transistor;  
a seventh capacitor coupled to the seventh transistor;  
an eighth transistor coupled to the seventh transistor; and  
an eighth capacitor coupled to the eighth transistor, wherein the sixth, seventh, and eighth transistors each have a lower threshold voltages than the first transistor at a common source voltage.

1 7. The charge pump circuit of claim 6 further comprising:  
2 a ninth transistor coupled to the eighth transistor;  
3 a ninth capacitor coupled to the ninth transistor;  
4 a tenth transistor coupled to the ninth transistor;  
5 a tenth capacitor coupled to the tenth transistor;  
6 an eleventh transistor coupled to the tenth transistor; and  
7 an eleventh capacitor coupled to the eleventh transistor, wherein the ninth,  
8 tenth, and eleventh transistors each have a lower threshold voltages than the first transistor at  
9 a common source voltage.

1 8. The charge pump circuit of claim 7 further comprising:  
2 a twelfth transistor coupled to the eleventh transistor;  
3 a twelfth capacitor coupled to the twelfth transistor;  
4 a thirteenth transistor coupled to the twelfth transistor;  
5 a thirteenth capacitor coupled to the thirteenth transistor, wherein the twelfth  
6 and thirteenth transistors each have a lower threshold voltages than the first transistor at a  
7 common source voltage.

1 9. The charge pump circuit of claim 8 further comprising:  
2 a fourteenth transistor coupled to the thirteenth transistor;  
3 a fourteenth capacitor coupled to the fourteenth transistor;  
4 a fifteenth transistor coupled to the fourteenth transistor; and  
5 an fifteenth capacitor coupled to the fifteenth transistor, wherein the fourteenth  
6 and fifteenth transistors each have a lower threshold voltages than the first transistor at a  
7 common source voltage.

1 10. The charge pump circuit of claim 3 wherein the first and third  
2 capacitors are coupled to receive a first clock signal, and the second and fourth capacitors are  
3 coupled to receive a second clock signal.

1 11. The charge pump circuit of claim 10 further comprising:  
2 a fifth capacitor coupled to the first transistor and a third clock signal;  
3 a sixth capacitor coupled to the second transistor and a fourth clock signal;  
4 a seventh capacitor coupled to the third transistor and the third clock signal;  
5 and

an eighth capacitor coupled to the fourth transistor and the fourth clock signal.

12. A method for receiving an input voltage and providing a boosted output voltage, the method comprising:  
increasing a first voltage at a first capacitor;  
coupling the first capacitor to a second capacitor through a first transistor;  
increasing a second voltage at the second capacitor; and  
coupling the second capacitor to a third capacitor through a second depletion transistor.

13. The method of claim 12 further comprising:  
increasing a third voltage at the third capacitor;  
coupling the third capacitor to a fourth capacitor through a third depletion transistor;  
increasing a fourth voltage at the fourth capacitor; and  
coupling the fourth capacitor to a fifth capacitor through a fourth depletion transistor.

14. The method of claim 13 further comprising:  
increasing a fifth voltage at the fifth capacitor;  
coupling the fifth capacitor to a sixth capacitor through a fifth depletion transistor;  
increasing a sixth voltage at the sixth capacitor; and  
coupling the sixth capacitor to a seventh capacitor through a sixth depletion transistor.

15. The method of claim 14 further comprising:  
increasing a seventh voltage at the seventh capacitor;  
coupling the seventh capacitor to a eighth capacitor through a seventh depletion transistor;  
increasing an eighth voltage at the eighth capacitor; and  
coupling the eighth capacitor to a ninth capacitor through a eighth depletion transistor.

16. The method of claim 15 further comprising:  
increasing a ninth voltage at the ninth capacitor;

3 coupling the ninth capacitor to a tenth capacitor through a ninth depletion  
4 transistor;  
5 increasing a tenth voltage at the tenth capacitor; and  
6 coupling the tenth capacitor to an eleventh capacitor through a tenth depletion  
7 transistor.

1 17. The method of claim 16 further comprising:  
2 increasing an eleventh voltage at the eleventh capacitor;  
3 coupling the eleventh capacitor to a twelfth capacitor through an eleventh  
4 depletion transistor;  
5 increasing a twelfth voltage at the twelfth capacitor; and  
6 coupling the twelfth capacitor to a thirteenth capacitor through a twelfth  
7 depletion transistor.

1 18. The method of claim 14 wherein the first transistor has a greater  
2 threshold voltage than the second, third, fourth, fifth and sixth transistors at a common source  
3 voltage.

1 19. The method of claim 13 further comprising:  
2 providing a first clock signal to the first and third capacitors; and  
3 providing a second clock signal to the second and the fourth capacitors.

1 20. The method of claim 19 further comprising:  
2 coupling a gate and a drain/source of the first transistor through a fifth  
3 transistor in response to the first clock signal;  
4 providing a third clock signal to fifth and sixth capacitors coupled to gates of  
5 the first and third transistors;  
6 coupling a gate and a drain/source of the second transistor through a sixth  
7 transistor in response to the second clock signal;  
8 providing a fourth clock signals to sixth and seventh capacitors coupled to  
9 gates of the second and fourth transistors; and  
10 coupling a gate and a drain/source of the third transistor through a seventh  
11 transistor in response to the first clock signal.

1 21. A charge pump circuit comprising:  
2 a first stage comprising a first depletion field-effect transistor;

3 a second stage comprising a second depletion field-effect transistor, the  
4 second stage being coupled to the first stage;  
5 a first capacitor coupled to the first stage; and  
6 a second capacitor coupled to the second stage.

1 22. The charge pump circuit of claim 21 further comprising:  
2 a third stage comprising a third depletion field-effect transistor, the third stage  
3 being coupled to the second stage;  
4 a fourth stage comprising a fourth depletion field-effect transistor, the fourth  
5 stage being coupled to the third stage;  
6 a third capacitor coupled to the third stage; and  
7 a fourth capacitor coupled to the fourth stage.

1 23. The charge pump circuit of claim 22 further comprising:  
2 a fifth stage comprising a fifth depletion field-effect transistor, the fifth stage  
3 being coupled to the fourth stage;  
4 a sixth stage comprising a sixth depletion field-effect transistor, the sixth stage  
5 being coupled to the fourth stage;  
6 a fifth capacitor coupled to the fifth stage; and  
7 a sixth capacitor coupled to the sixth stage.

1 24. The charge pump circuit of claim 23 further comprising:  
2 a seventh stage comprising a seventh depletion field-effect transistor, the  
3 seventh stage being coupled to the sixth stage;  
4 an eighth stage comprising an eighth depletion field-effect transistor, the  
5 eighth stage being coupled to the seventh stage;  
6 a seventh capacitor coupled to the seventh stage; and  
7 an eighth capacitor coupled to the eighth stage.

1 25. The charge pump circuit of claim 24 further comprising:  
2 a ninth stage comprising a ninth field-effect transistor, the ninth stage being  
3 coupled to the eighth stage;  
4 a tenth stage comprising a tenth depletion field-effect transistor, the tenth stage  
5 being coupled to the ninth stage;

an eleventh stage comprising an eleventh field-effect transistor, the eleventh stage being coupled to the tenth stage;

a ninth capacitor coupled to the ninth stage;

a tenth capacitor coupled to the tenth stage; and

an eleventh capacitor coupled to the eleventh stage.

26. The charge pump circuit of claim 22 wherein the first and third capacitors are coupled to receive a first clock signal, and the second and fourth capacitors are coupled to receive a second clock signal.

91 27. The charge pump circuit of claim 26 further comprising:  
a fifth capacitor coupled to a gate of the first depletion transistor;  
a sixth capacitor coupled to a gate of the second depletion transistor;  
a seventh capacitor coupled to a gate of the third depletion transistor; and  
an eighth capacitor coupled to a gate of the fourth depletion transistor, wherein the fifth and seventh capacitors are coupled to receive a third clock signal, and the sixth and eighth transistors are coupled to receive a fourth clock signal.

28. The charge pump circuit of claim 27 further comprising:  
a fifth transistor coupled across two terminals of the first transistor and to the first capacitor;  
a sixth transistor coupled across two terminals of the second transistor and to the second capacitor;  
a seventh transistor coupled across two terminals of the third transistor and to the third capacitor; and  
an eighth transistor coupled across two terminals of the fourth transistor and to the fourth capacitor.

29. An integrated circuit comprising:  
programmable logic circuitry; and  
a charge pump circuit comprising:  
first and second stages coupled together,  
a first capacitor coupled to the first stage, and  
a second capacitor coupled to the second stage, wherein the second stage comprising a depletion transistor.